Single-Chip SiGe Transceiver Chipset for V-band Backhaul Applications from 57 to 64 GHz

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1 Introduction

The smartphone revolution has led to a growing demand in mobile data traffic which subsequently has resulted in increased throughput per user. The high mobile data requirements has led to the deployment of advanced 4G services like Long Term Evolution (LTE) by the mobile network operators and this is expected to grow further in the coming years. LTE and LTE Advanced will provide users with higher data rates which will increase data traffic drastically. The increasing data rate puts an enormous burden on the network operator’s backhaul networks. The bulk of today’s basestation infrastructure is not ready to support the required high data throughput using the existing microwave backhaul techniques. The connection between the basestations is usually planned for lower data rates up to 100 MBit/s which has to be increased significantly to meet the demands for LTE systems. Though optical fiber based backhaul networks can handle a huge data throughput, they are faced with the challenge of easy and cost-effective deployment. The concept of small cells make the deployment of fiber optic based solution even complex and expensive and sometimes even not feasible. This is where the wireless backhaul technology comes into place. A new solution using millimeter wave backhaul opens upto 10 GHz bandwidth in the E-band (71-76 and 81-86 GHz) and 7 GHz bandwidth in the V-band (57–64 GHz). The high bandwidth and channel spacing offered at these frequencies enables data rates higher than 1 Gbps for video and data service even with simple modulation schemes.

Infineon has developed a complete family of packaged RF Transceivers for mobile backhaul applications – supporting both the V-band and E-band frequencies with its BGT60, BGT70 and BGT80 ICs. The modular approach followed by Infineon provides same package dimensions and RF footprint for all the three chipsets which enable customers to quickly setup a radio system at any of the above allowed frequency bands. The highly integrated ICs help to eliminate discrete components, thereby simplifying the customer’s system design and time-to-market. This also helps to reduce the total cost of the mmWave backhaul solutions.

The ICs are designed in Infineon´s advanced SiGe:C (Silicon Germanium) technology with device transit frequency of 200 GHz, that enable integration of several mmWave building blocks such as Power Amplifier (PA), Low Noise Amplifier (LNA), Up- and Down-Convertor, Programmable Gain Amplifier (PGA), Voltage Controlled Oscillator (VCO) and more with high performance into a single chip. This technology is proven and fully qualified for other Infineon millimeter- and microwave chipsets already. Furthermore, Infineon is the leading company to house these single chipsets into a plastic Embedded Wafer Level Ball Grid Array (eWLB) package which can be processed in standard SMT flow.

In this application note, the performance of Infineon’s fully integrated V-Band Transceiver BGT60 for 57 to 64 GHz on its evaluation board is described in detail.

All the measurements presented in this application note are done port-to-port on Infineon’s EVB i.e. Board losses (~2dB) are not dembedded. The measurements are done at backside chip temperature of 45°C. This also causes loss of additional 1dB. For the specifications of BGT60 transceiver IC, please refer the datasheet of BGT60.

2 About V-Band Backhaul Application

Solutions using millimeter wave backhaul in the V-Band of 57-64 GHz open up 7 GHz bandwidth for a full-duplex wireless radio link. It allows gigabit data rates with the simplest modulation scheme which minimize linearity requirements of the transmitter power amplifier (PA). With more spectrally efficient modulations, data rates even higher than 10 Gbps can be achieved. Antennas at high frequencies become compact and can provide higher gain than their contemporaries at lower microwave frequencies which can help improve the link condition.

A number of requirements for V-Band communication are specified by ETSI within the document **ETSI 302 217-3** "*Fixed Radio Systems; characteristics and requirements for point-to-point equipment and antennas; Part 3: Equipment operating in frequency bands where both frequency coordinated or uncoordinated deployment might be applied; Harmonizing EN covering the essential requirements of the article 3.2 of the R&TTE directive"*. The high atmospheric attenuation around the 60 GHz band due to oxygen absorbtion helps to provide a strong immunity to interference and allows a higher frequency reuse. The ETSI specifications recommend a minimum antenna gain of 30 dBi. For the radio channel arrangements and nominal bandwidth, two different alternatives are considered. The first alternative is defined as "Free system bandwidth, occupying up to the whole band" and In the second case the maximum channel bandwidth is limited to 2.5 GHz with the channel selection defined as (n*50 MHz), where n = [1….50]. Maximum equivalent isotropically radiated power (EIRP) is specified to 55 dBm and a maximum transmitter output power of +10 dBm is specified.

A large channel bandwidth with a higher modulation scheme eventually demands higher carrier-to-noise ratio (CNR) which imposes stringent requirements on the high frequency transmitter and receiver design. For example, a typical receiver with 12dB noise figure at the antenna port in a V-Band radio system using 500MHz channel bandwidth and 16-QAM modulation would need about the same minimum receiver signal power level as a system using 1250 MHz BW and FSK to ensure the bit error rate (BER) of 1E-6.

The radio link can be either in full-duplex (FDD) or half-duplex (TDD) system configuration. In a FDD V-Band system, any two blocks of frequencies between 57-64 GHz are used for transmission or reception, depending upon the availability of Diplexers. In a TDD system, one BGT60 chip is installed on each side of the link stations. Each chip in a base station can work in the TX or RX mode independently.

3 Infineon V-Band BGT60 RF Front-End Transceiver Chipset

3.1 Key Features

- BGT60 covers the V-Band frequency range from 57 to 64 GHz
- Fabricated with Infineon's advanced Silicon-Germanium (SiGe) technology
- Housed in Infineon's **E**mbedded **W**afer **L**evel **B**all-Grid Array (eWLB) **P**ackage
- BGT60 can be programmed via SPI interface to work either in transmit (TX) or/and receive (RX) mode
- Zero IF – differential I/Q interface – direct conversion architecture
- Differential RF transmit output signaling
- Differential RF receive input signaling
- Differential intermediate frequency I/Q signaling
- Peak detector at VGA input at transmit path
- Peak detector at PA output at transmit path
- Built-in temperature sensor
- SPI interface
- ESD protected device
- BITE (**B**uilt-**I**n-**T**est **E**quipment) for self-test and calibration in production at Infineon to verify RF performance
- Can support TDD or FDD systems

Applications:

- V-Band from 57 to 64 GHz FDD or TDD systems for telecommunication applications

Product Name	Package	Marking
BGT60	PG-WFWLB-119-1	BGT60TR11

3.2 Description of BGT60

Currently, different mmWave system implementations based on III/V-compound semiconductor, silicon bipolar or silicon CMOS technologies have been reported. The advancements in SiGe based technologies in the last years have resulted in their increased use for applications in the mmWave regime with their successful deployment in several existing commercial mmWave applications. Infineon has a long history of research & development with SiGe based technologies and the BGT60 transceiver IC is designed with one of Infineons in-house advanced SiGe bipolar process.

The single-chip transceiver chipset BGT60 is manufactured with Infineon's 200 GHz-f_T SiGe-technology and applicable for telecommunication applications in the microwave and mmWave range. Infineon's 200 GHz Silicon Germanium (SiGe) technology is proven and qualified for Millimeter (e.g. 77 GHz automotive radar) and Microwave chipsets (e.g. 24 GHz automotive/industrial radar). BGT60 uses fully-differential direct conversion architecture for the transmitter and receiver. A Fully-differential (balanced) architecture helps to mitigate the effects of common-mode interference and RF grounding issues, which become extremely critical at higher operating frequencies. Also a differential architecture offers the advantage of reduced even-order harmonics.

The direct conversion architecture simplifies the frequency up/down-conversion process and can reduce bulky and expensive off-chip filtering components. Through the direct conversion architecture of the transceiver, the interface between RF and baseband is simplified significantly compared to currently available discrete millimeter wave solutions. Furthermore, the offering of the single chip solution in a eWLB plastic package makes a major difference to the market. With the packaged chipset, customers can save cost and reduce the time-to-market significantly.

The outstanding RF performance of SiGe technology – such as deliverable saturated output power of up to 14.5 dBm, a low receiver noise figure of 8 dB and excellent VCO phase noise performance better than -83 dBc/Hz at 100kHz offset – allow designers to implement systems with high modulation schemes up to QAM64 with a sample rate of more than 1 Giga Samples per second (GS/s) or simple systems with QPSK with large bandwidth through channel aggregation. ESD (Electrostatic Discharge) performance of more than 1 kV increases robustness. The low power consumption of less than 2 W for this backhaul transceiver family also allows network operators to reduce related fixed expenses.

In general, Infineon's single-chip V-Band transceiver offers customers the following advantages:

- lower production cost
- broadband high data rate telecommunication which enable Gbps radio link
- compact single chip integration leading to much smaller form factor
- excellent device performance
- individual VCO centering taking into account process and temperature variation
- robust design & insensitivity to interference through direct conversion architecture and fully differential topology
- standard plastic package allows industrial assembly and cleaning tool to be used
- product family approach with the same foot print i.e. same PCB layout possible for E-Band radios

4 Typical Measurement Results

In Chapter 4, typical measurement results of the V-Band 57 to 64 GHz transceiver, BGT60 are summarized. Please note that these measurements are performed **on the Infineon evaluation board at room temperature**.

Table 1 Measurement Results - DC Parameters

Parameter	Symbol	Unit	Value	Condition
Voltage Supply	Vcc	V	3.300	
Current Consumption - IC powered on, TX off, RX off - TX on, RX off - TX off, RX on - TX on, RX on	 ICoff ICTX ICRX ICTRX	mA	 323 550 428 635	 @ max power @ max power

The current values are of complete EVB. For BGT60 current consumption only please refer Datasheet.

Table 2 IF Port Features and Sensor Characteristics

Parameter	Symbol	Unit	Value	Condition
Output Power Vs PA Peak Detector Readout Relation * PPD_PA selected via MUXout * This provides the output power level at the landing pad	Pout PPD_PA (MUX out)	dBm V	$Pout = t_1 * \ln(\frac{PPD\_PA - y_0}{A_1})$ $y_0 = 0.8829$ $A_1 = 0.1867$ $t_1 = 7.9737$	
Temperature Sensor Sensitivity	Tsense	mV/K	5	
Load Impedance for Tsense Output	$Rsens_{load}$	MΩ	1	single-ended
IF Input Interface at TX				
Signaling				differential
IF Load Impedance	IFload	Ω	100	differential
IF Bandwidth	IFBW	MHz	500	
IF Lower Cutoff Frequency	IFlow	kHz	3	external Capacitance > 1µF required
IF Higher Cutoff Frequency	IFhigh	MHz	500	
IF Coupling on Board			AC	value to be specified
IF Output Interface at RX				
Signaling				differential
IF Load Impedance	IFload	Ω	400	Differential, minimum value
IF Bandwidth	IFBW	MHz	500	
IF Lower Cutoff Frequency	IFlow	kHz	3	external Capacitance > 1µF required
IF Higher Cutoff Frequency	IFhigh	MHz	500	
IF Coupling on Board			AC	value to be specified
I/Q Amplitude Imbalance	IQAI	dB	0.5	
I/Q Phase Imbalance	IQPI	deg	2	

Table 3 Measurement Results - Transmitter

Parameter	Symbol	Unit	Value			Condition
Frequency	Freq	GHz	57	60	64	
TX Output						
Output Signaling				differential		
TX-Port Load Impedance	TX_{load}	Ω		100		differential
TX Chain Gain	G_{TX}	dB	24	29	33	From one IF port to Waveguide port
Output Referred P-1dB	$OP\text{-}1dB_{TX}$	dBm	9	11.5	11.5	differential 100 Ω load
Saturated Power	P_{sat}	dBm	11.6	15	14.6	differential 100 Ω load
Output Referred IP3	$OIP3_{TX}$	dBm	16.9	20.3	15.7	differential 100 Ω load
PA Control Dynamic Range	P_ctrl_d	dB		11.7		
LO feed-through Suppression	LO_s	dBc		-57		before LO calibration
PA Control Step	P_ctrl_s	dB		0.1 to 2		6 bits
Image Rejection	IMR	dBc		20		w/o feedback loop

Table 4 Measurement Results – LO Generation

Voltage Control Sensitivity	Kvco	GHz/V	5	2.2	1	@TX output
Phase Noise						
@100kHz Offset	$PN_{ssb100k}$	dBc/Hz	-81	-83.6	-85	SSB
@1MHz Offset	PN_{ssb1M}	dBc/Hz	-101	-103.8	-105	SSB
@10MHz Offset	PN_{ssb10M}	dBc/Hz	-122	-124.2	-126	SSB
Divider Output Power	$PDIV_{out}$	dBm		-9		differential 100 Ω load
VCO Tuning Voltage	V_{tune}	V	0		5.5	single tuning port

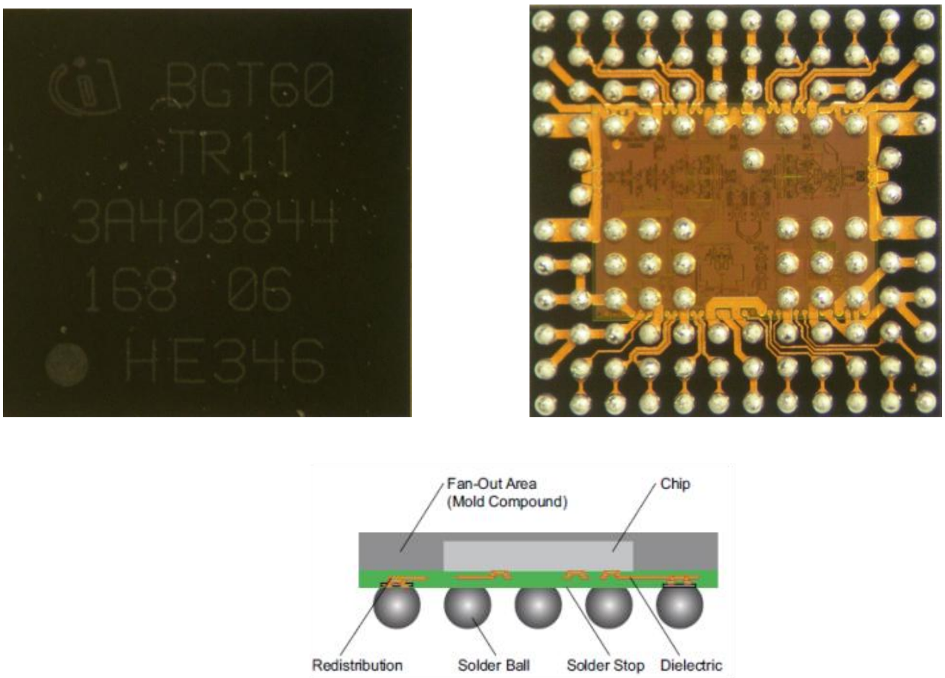
Table 5 Measurement Results - Receiver

Parameter	Symbol	Unit	Value			Condition
Frequency	Freq	GHz	57	60	64	
RX Chain						
Input Signaling						differential
Conversion Gain	CG_{diff}	dB	17.4	20	22.9	differential in **400Ω** load at IF Ports
Double-Side-Band Noise Figure	NFdsb	dB	8.4	8	7.1	
Input Referred P-1dB	$IP\text{-}1dB_{RX}$	dBm	-11	-12.5	-13.5	
Input Referred IP3	$IIP3_{RX}$	dBm	-2.9	-3.5	-4.9	
LO Residual Power at the RX Input	LO_{res}	dBm		-52		
RF-Port Load Impedance	RF_{load}	Ω		100		differential

5 Package

5.1 BGT60 in PG-WFWLB-119-1 Package

The BGT60 chipset is in eWLB type package PG-WFWLB-119-1 with bump balls of 300µm diameter and 150µm height as shown in **Figure 1**. The physical dimension of 6.0 x 6.0 mm² with a bump pitch of 500 µm is shown in **Figure 2**. The maximum height of the package is 0.8 mm with 0.1 mm max planarity variation. The maximum variation of bump coplanarity is 80 µm. On top of the package, Pin 1 is marked by a laser marking. The product name and its production date code are also described there.



Package Dimension: 6.0 mm x 6.0 mm x 0.8 mm

Figure 1 Top View (left), Bottom View (right) and Side View of BGT60 in eWLB Package

For mmWave applications, eWLB offers excellent electrical and thermal characteristics. With a well-engineered design, it offers a comparable loss like a bonding wire package version but has large bandwidth which is required for broadband mmW applications. Furthermore, its outstanding thermal resistance of 15 K/W ensures its proper working even under critical environment. The BGA-like package form enables customers to use industrial standard reflow process to solder it.

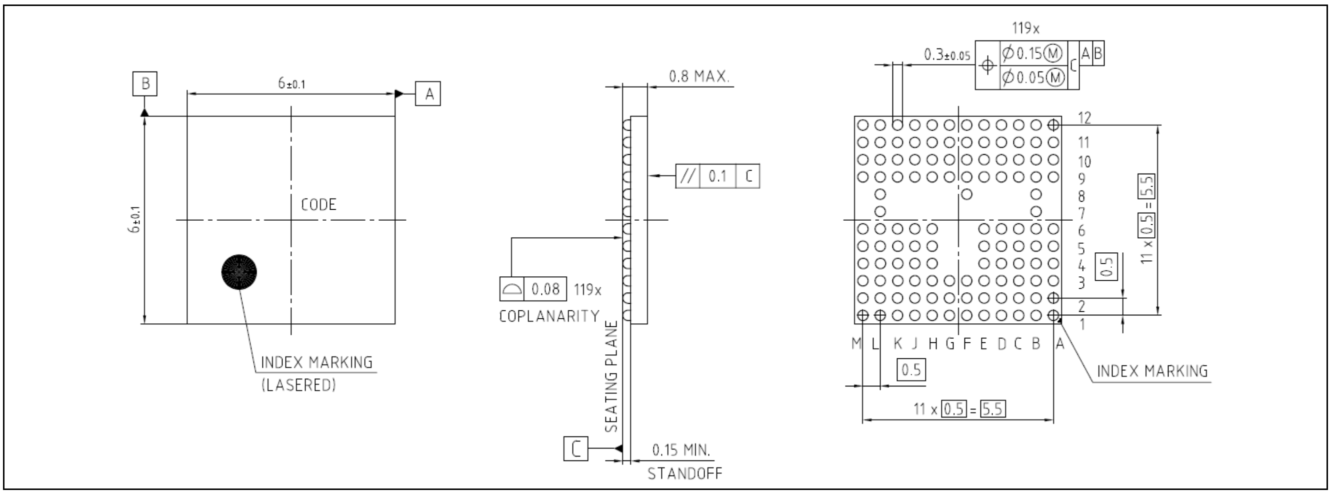


Figure 2 Dimension of eWLB Package PG-WFWLB-119-1 for BGT60 (left: top view; center: side view; right: bottom view)

5.2 Pin Definition and Function

Figure 3 shows the top view of BGT60 package eWLB PG-WFWLB-119-1 with the pin number assignment. The function of each pin is described in **Table 6** below.

The ground pins (in black color) are used not only for RF and DC but also as a heat sinker for the BGT60 chipset on the PCB. It has to be noted that the four edge ground pins A1, A12, M1 and M12 are in fact not used in the transceiver IC but it is recommended to connect them to the RF ground for mechanical stability.

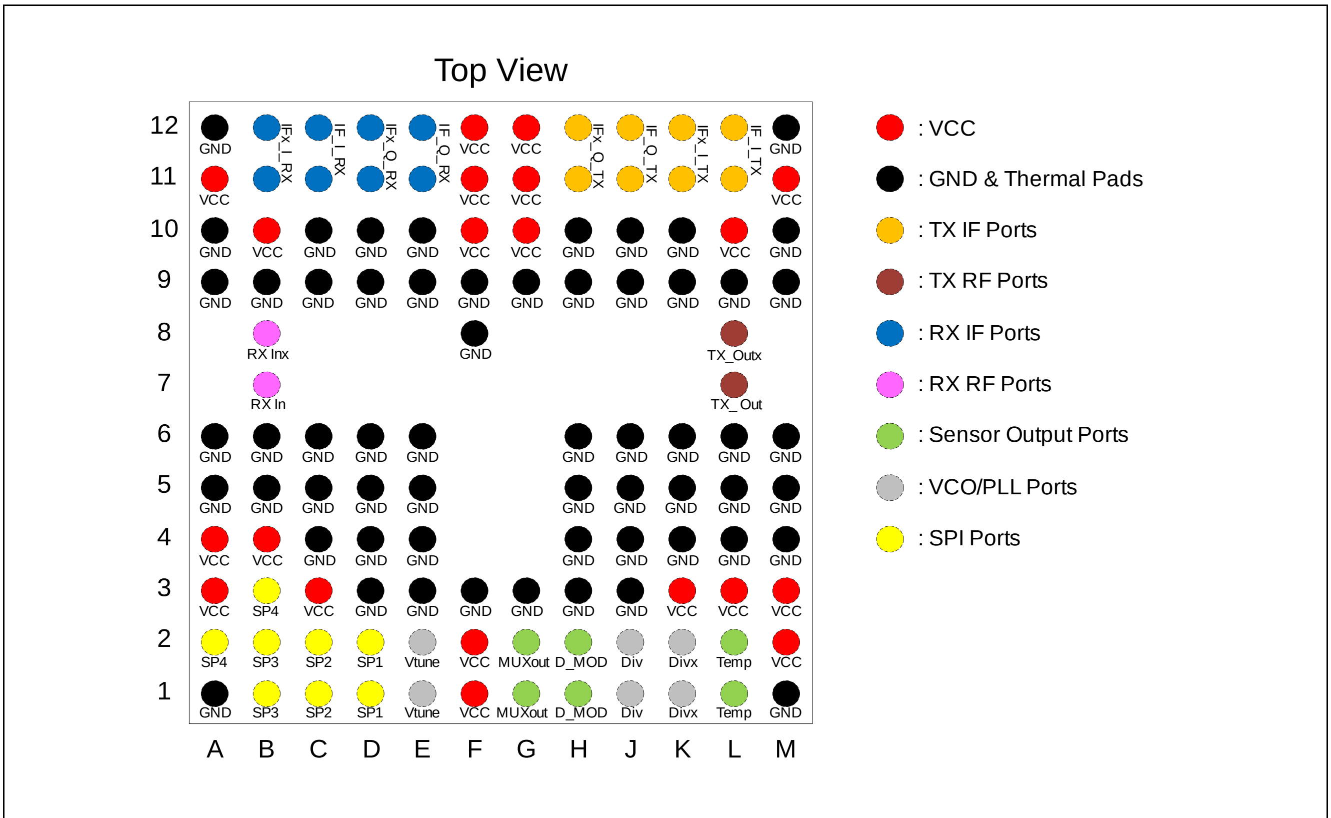


Figure 3 Pin Number Assignment of BGT60 package eWLB PG-WFWLB-119-1 (Top View)

Table 6 Pin Definition and Function

Pin No.	Name	Function
A3, A4, A11, B4, B10, C3, F10, F11, F12, G10, G11, G12, L10, M11	Vcc	DC supply for the transceiver chip – 3.3V
K3, L3, M2, M3	Vcc_Temp	Supply voltage for the temperature sensor – 3.3V
F1, F2	Vcc_VCO	Supply voltage for the VCO – 3.3V
E1, E2	Vtune	VCO tuning voltage
D1, D2	SP1	SPI Enable - chip select
C1, C2	SP2	SPI Dataout - SPI data sequence (device → control board)
B1, B2	SP3	SPI Data - SPI data sequence (control board → device)
A2, B3	SP4	SPI clock
G1, G2	MUXout	MUX output (PPD_PA or PPD_MOD DC level output)
H1, H2	D_MOD	Modulator detector output
L1, L2	Temp	Temperature sensor output – DC voltage
J1, J2	Div	Frequency divider output
K1, K2	DivX	Complementary frequency divider output
B7	RX_In	RF input of receiver
B8	RX_Inx	Complementary RF input of receiver
B11, B12	IFx_I_RX	Complementary inphase IF output of receiver
C11, C12	IF_I_RX	Inphase IF output of receiver
D11, D12	IFx_Q_RX	Complementary Quadrature IF output of receiver
E11, E12	IF_Q_RX	Quadrature IF output of receiver
L7	TX_Out	RF output of transmitter
L8	TX_OuTX	Complementary RF output of transmitter
L11, L12	IF_I_TX	Inphase IF input of transmitter
K11, K12	IFx_I_TX	Complementary inphase IF input of transmitter
J11, J12	IF_Q_TX	Quadrature IF input of transmitter
H11, H12	IFx_Q_TX	Complementary Quadrature IF input of transmitter
A5, A6, A9, A10, B5, B6, B9, C4, C5, C6, C9, C10, D3, D4, D5, D6, D9, D10, E3, E4, E5, E6, E9, E10, F3, F8, F9, G3, G9, H3, H4, H5, H6, H9, H10, J3, J4, J5, J6, J9, J10, K4, K5, K6, K9, K10, L4, L5, L6, L9, M4, M5, M6, M9, M10	GND	Ground and thermal pads
A1, A12, M1, M12	GND	A1, A12, M1, M12 are electrically not connected in chip but should be connected to ground for mechanical stability.

Note: all pins described in the same line need to be connected on the PCB.

6 BGT60 Evaluation Board

6.1 Overview of BGT60 Evaluation Board

Figure 4 shows the top view of the evaluation board for BGT60. In addition to the BGT60 chip, the PLL circuit with a reference oscillator is also implemented on the evaluation board as shown in **Figure 4**.

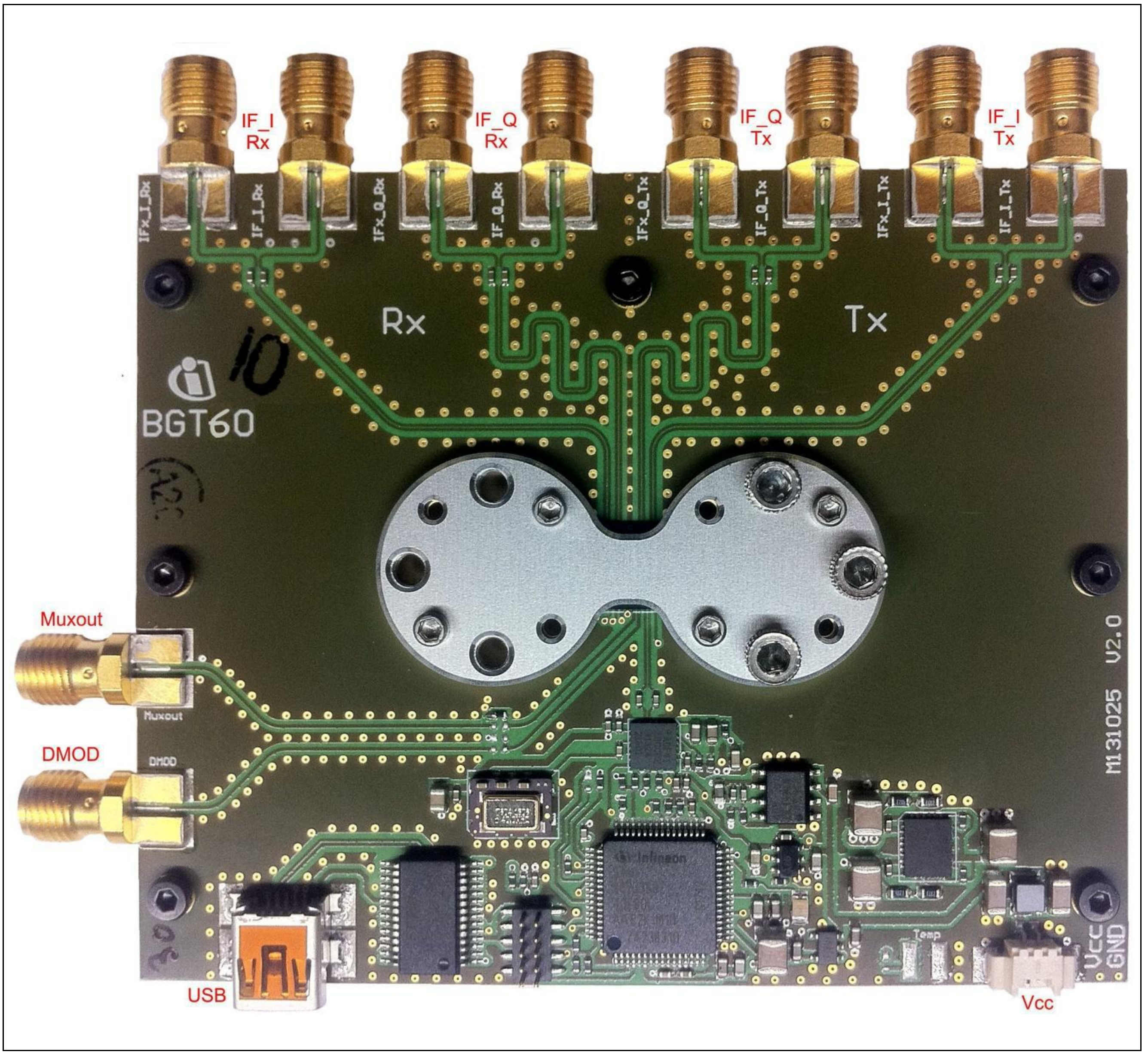


Figure 4 Evaluation Board for BGT60 – Top View

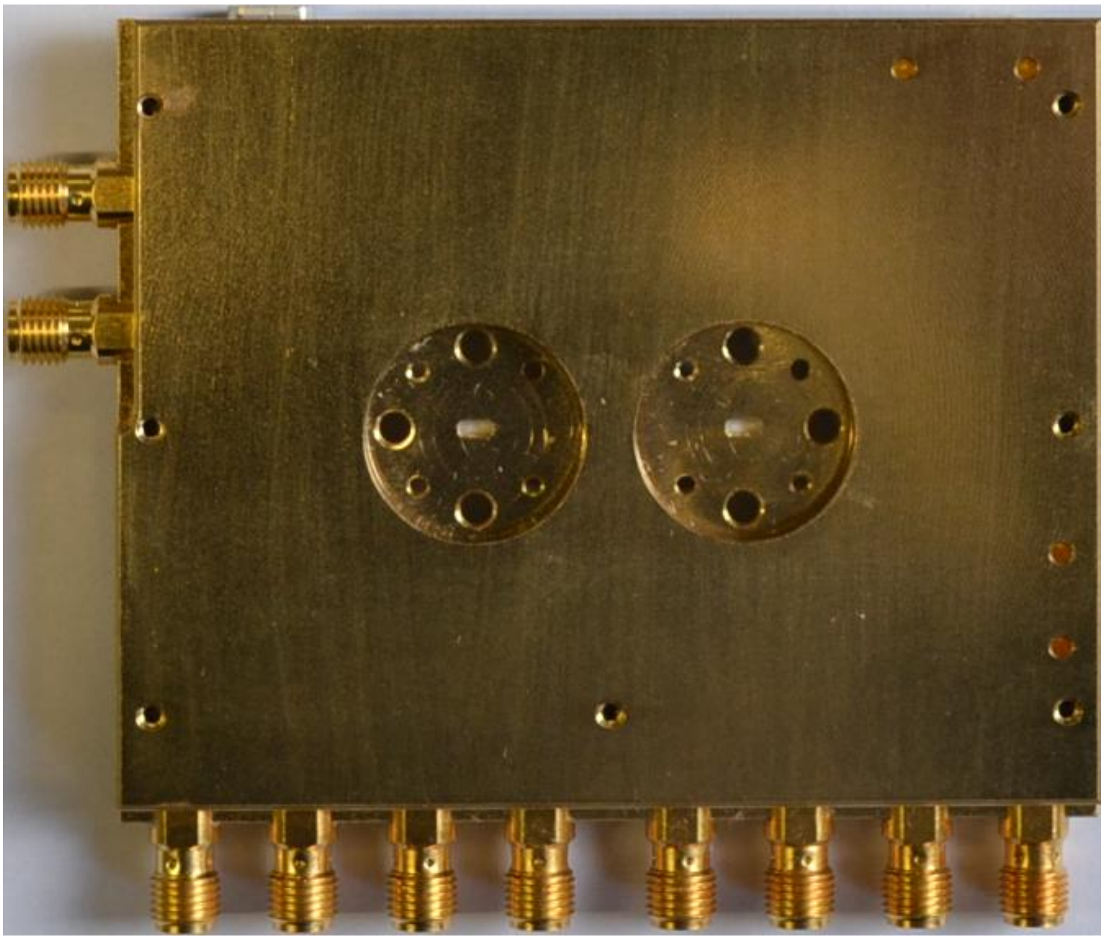


Figure 5 Evaluation Board for BGT60 – Bottom View

Table 7 Interface Description of BGT60 Application Board

Pin	Function	Description
SMA Connectors		
DMOD	Wideband PPD MOD output	Envelop tracking detector
Muxout	Provides DC voltage corresponding to PPD PA or PPD MOD	PPD PA or PPD MOD selectable through SPI control
IF_I_TX/ IF_Ix_TX	Inphase/Complementary I input of transmitter	Source impedance at input: differential 100 Ω
IF_Q_TX/ IF_Qx_TX	Quadrature/Complementary Q input of transmitter	Source impedance at input: differential 100 Ω
IF_I_RX/ IF_Ix_RX	Inphase/Complementary I output of receiver	Load impedance at output: differential 400 Ω
IF_Q_RX/ IF_Qx_RX	Quadrature/Complementary Q output of receiver	Load impedance at output differential 400 Ω
RF interface		
TX/RX Port	Transmitter/Receiver WR-15 waveguide	WR-15 waveguide

7 Performance of BGT60 Transmitter

The output spectrum at the TX port of BGT60 is shown in **Figure 6**. The measurement setup is shown in **Figure 7**. A Direct Digital Synthesizer (DDS) from Analog Devices (AD9959) is used to generate the IF signals for the transmitter. By adjusting the phase of the I and Q output signals from the DDS an image rejection greater than 50 dBc is achieved at the transmitter output. A V-band smart harmonic mixer is used to measure the output signal. The transmitter output power level is kept low by setting the DAC VGA value to 27 in order not to drive the smart harmonic mixer in compression. The carrier feedthorugh suppression is achieved by sweeping the values of DAC_MOD_I and DAC_MOD_Q registers. LO suppression of >50dB is achieved with this particular setup.

Figure 8 shows the linear and saturated output power at the transmitter output between 57-64 GHz. The transmitter gain over frequency is plotted in **Figure 9**. **Figure 10** shows the measured output 1-dB compression point over frequency. **Figure 11** shows the measured third order intermodulation performance of the transceiver over frequency. The transmitter output power can be varied by changing the DAC VGA and enabling/disabling the VGA buffer. **Figure 12** shows the transmitter performance vs different DAC VGA settings.

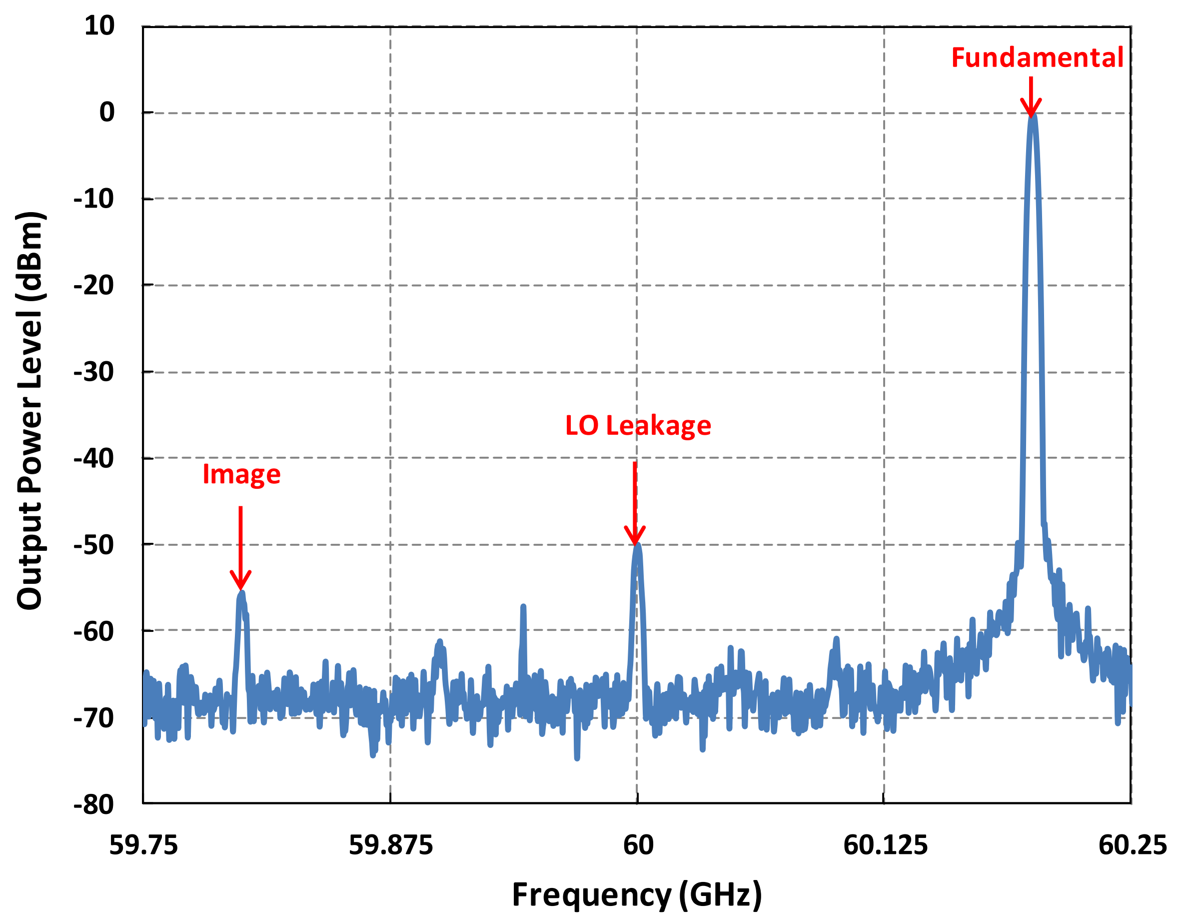


Figure 6 Output Spectrum of BGT60 at TX Waveguide Port on the evaluation board @ f_{TX}=60.22 GHz (DAC VGA=27)

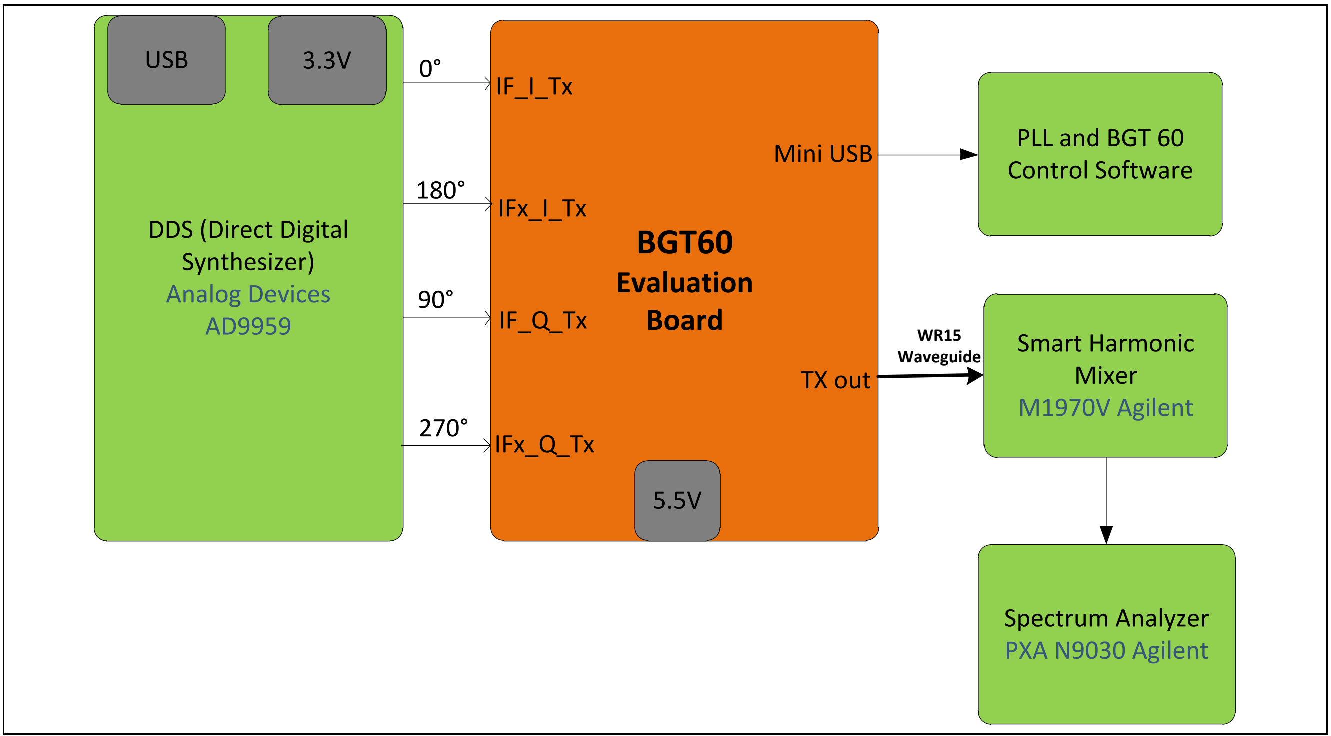


Figure 7 Measurement Setup used to measure TX Output Spectrum of BGT60 @ f_{TX}=60.2 GHz

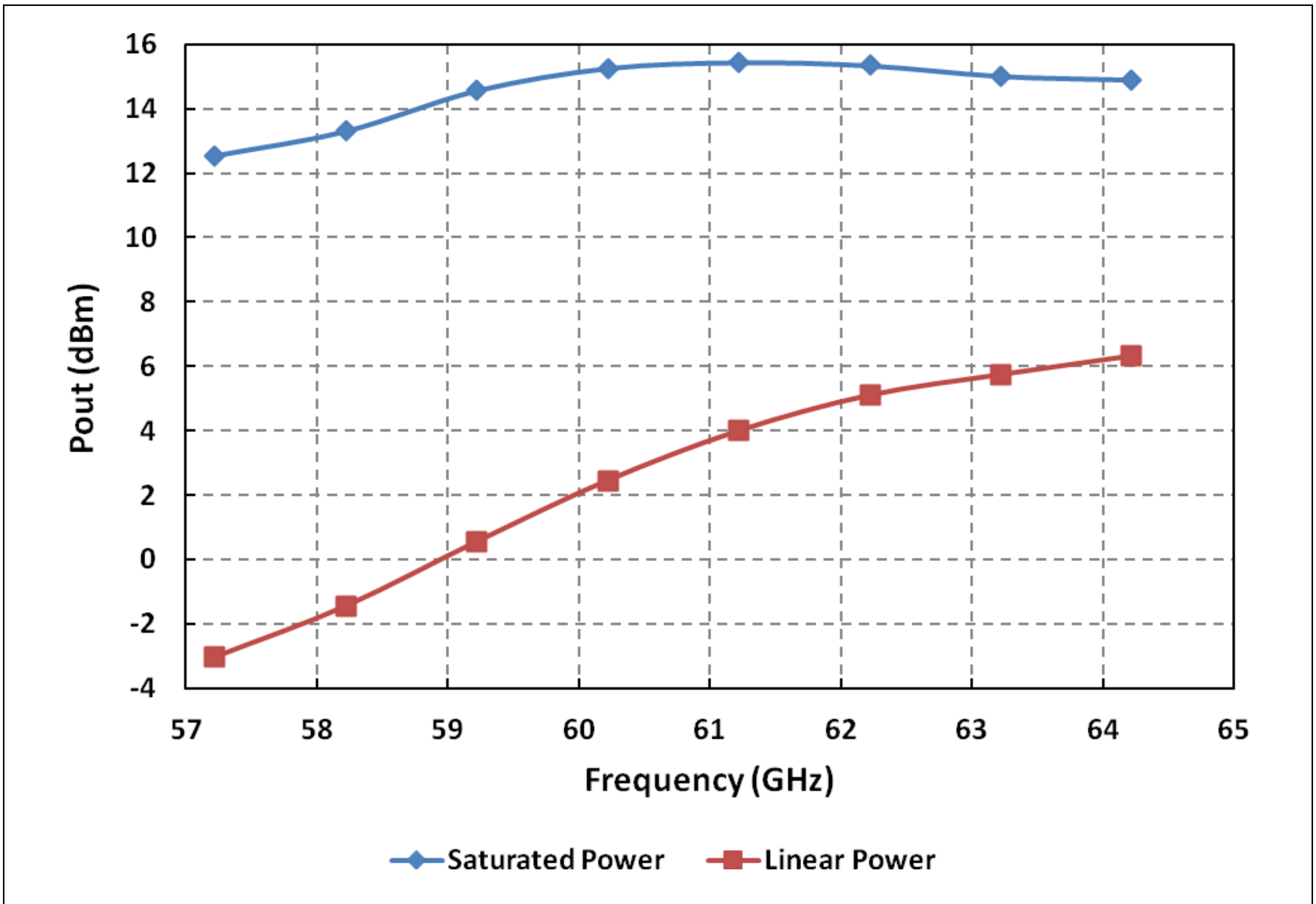


Figure 8 Linear ($P_{IF/TX}$=-27 dBm) and Saturated Power variation over Frequency of BGT60 (DAC VGA=63)

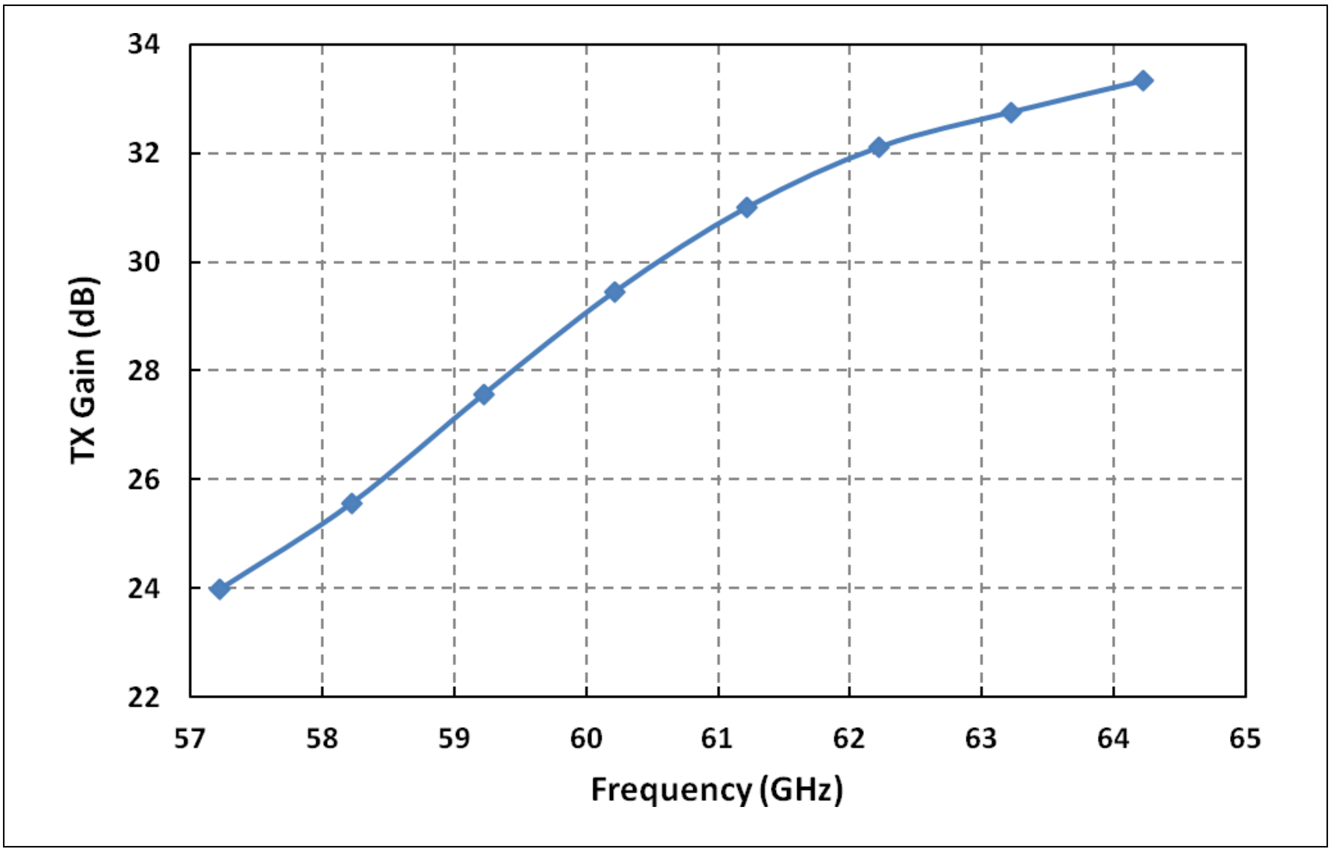


Figure 9 Linear Gain ($P_{IF/TX}$=-27 dBm) over Frequency @ DAC VGA=63

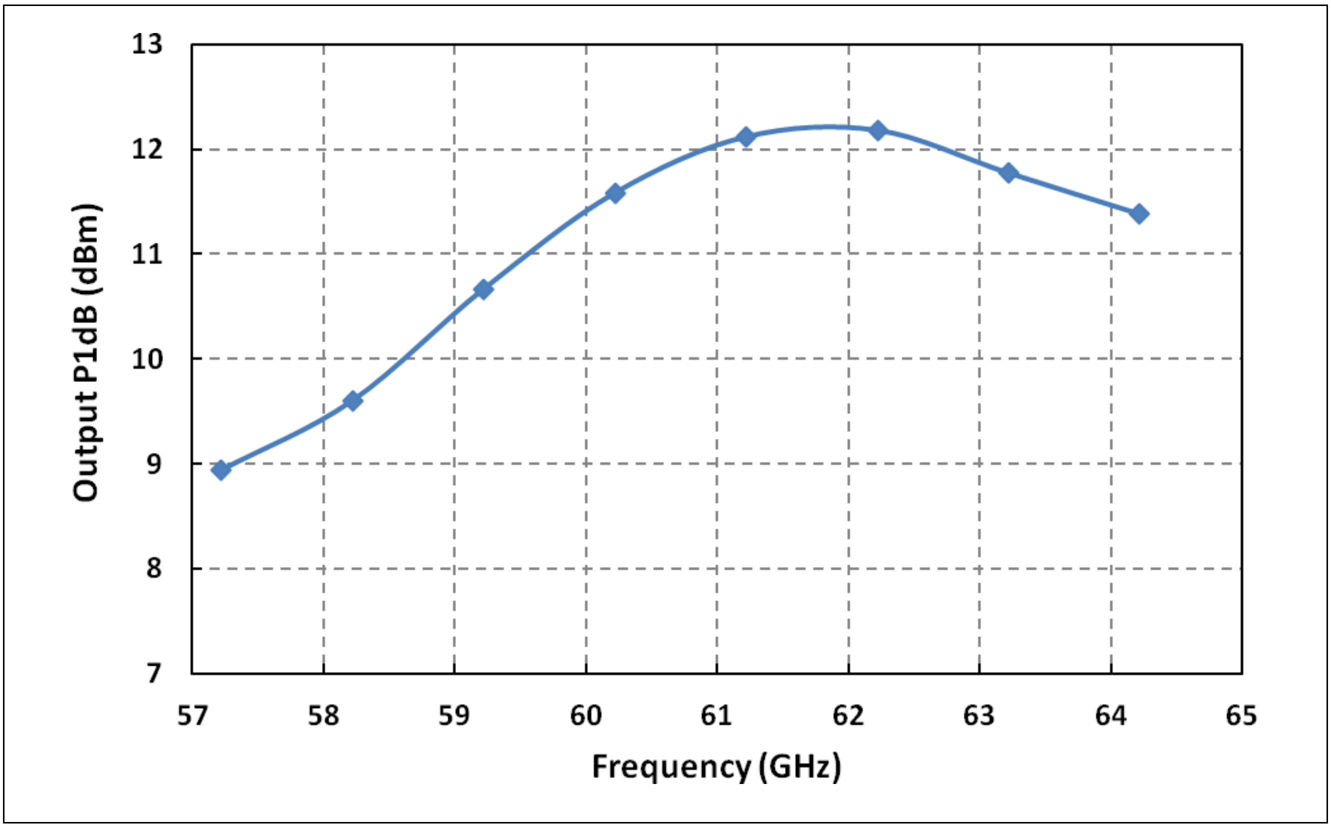


Figure 10 Output P1dB over Frequency @ DAC VGA=63

7.1 Measurement Results of 3rd-Order Intermodulation Products

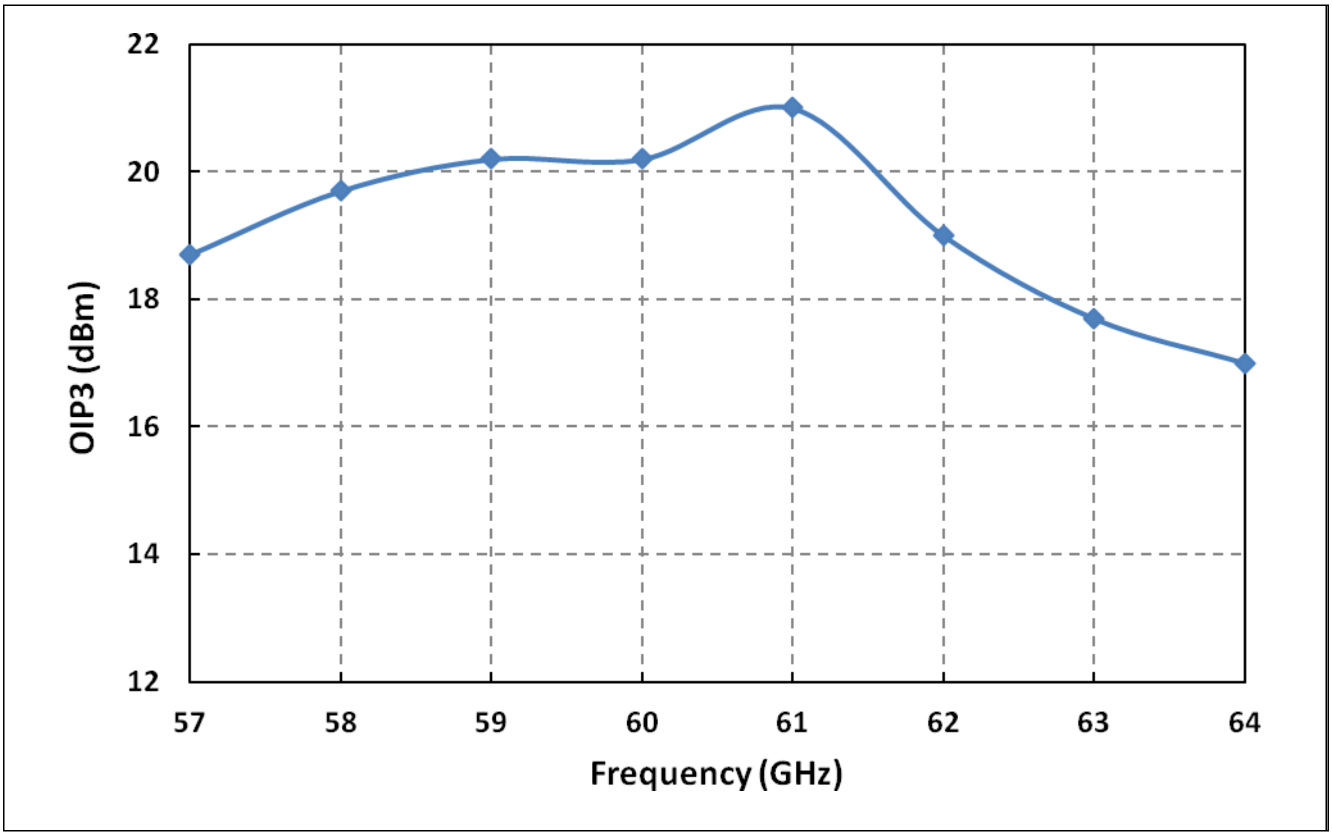


Figure 11 OIP3 versus Frequency at IF Input Power Level=-27 dBm

7.2 Measurement Results of VGA and Buffer Amplifier

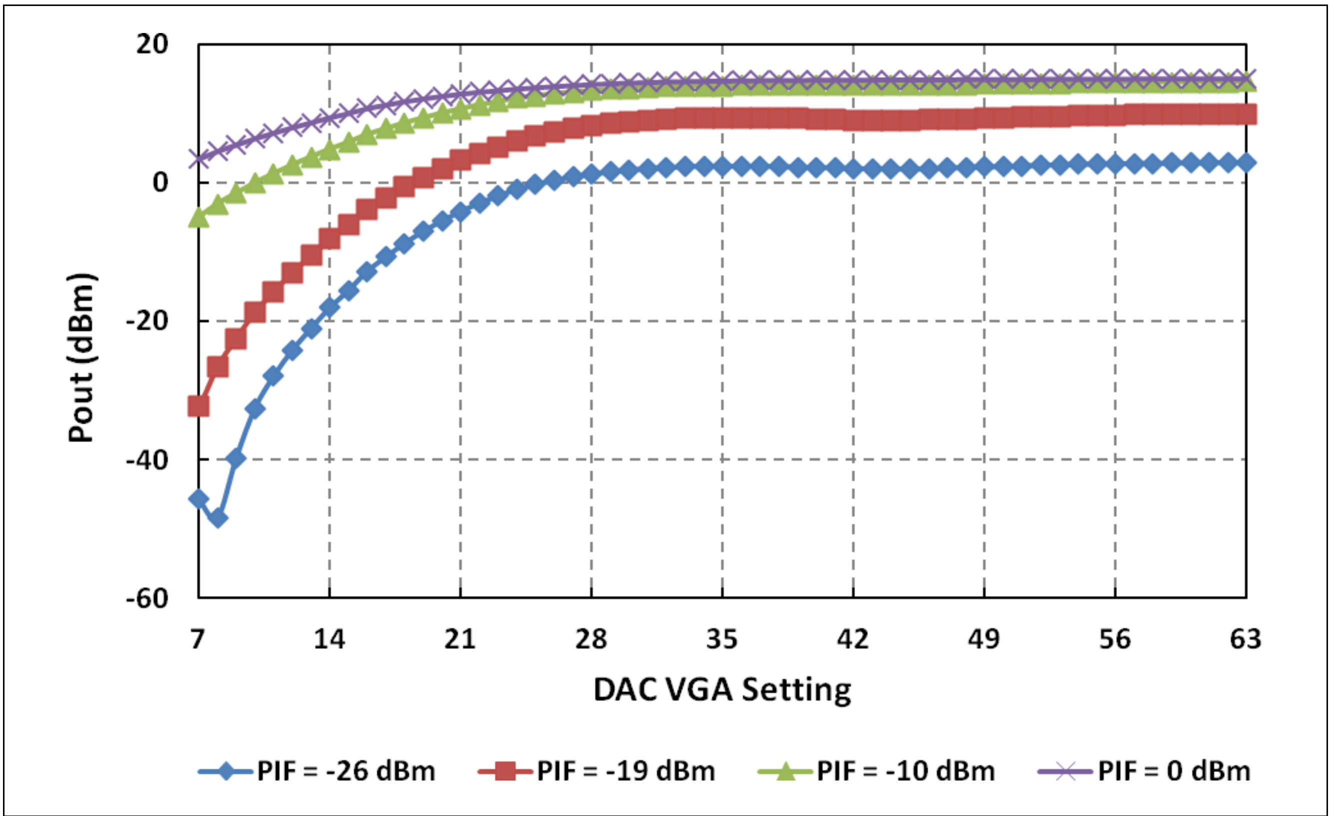


Figure 12 DAC VGA Setting versus Output Power at different IF Input Power levels (f_{TX} = 60.22 GHz)

7.3 PPD Power Amplifier – MUX out

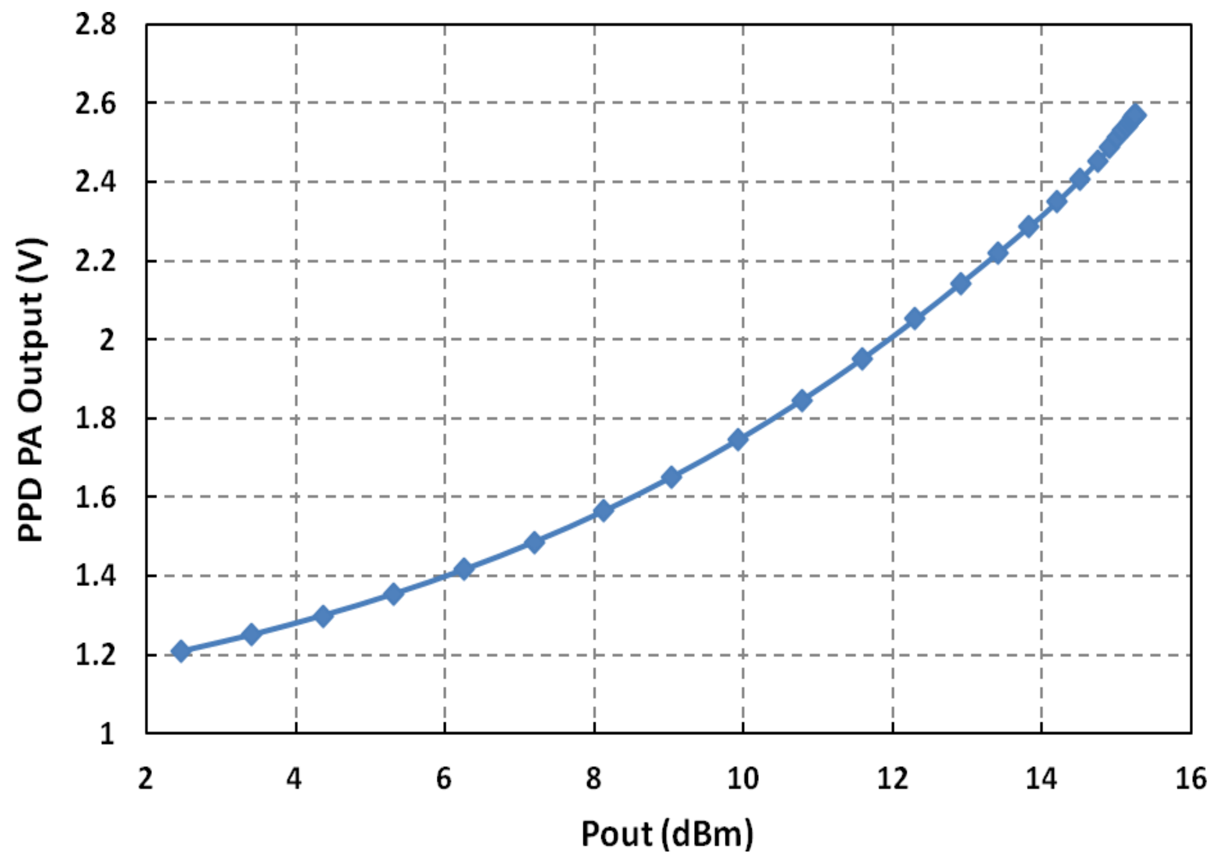


Figure 13 PPD PA Output Voltage versus Output Power @ f_{TX}=60.22 GHz

8 Performance of BGT60 Receiver

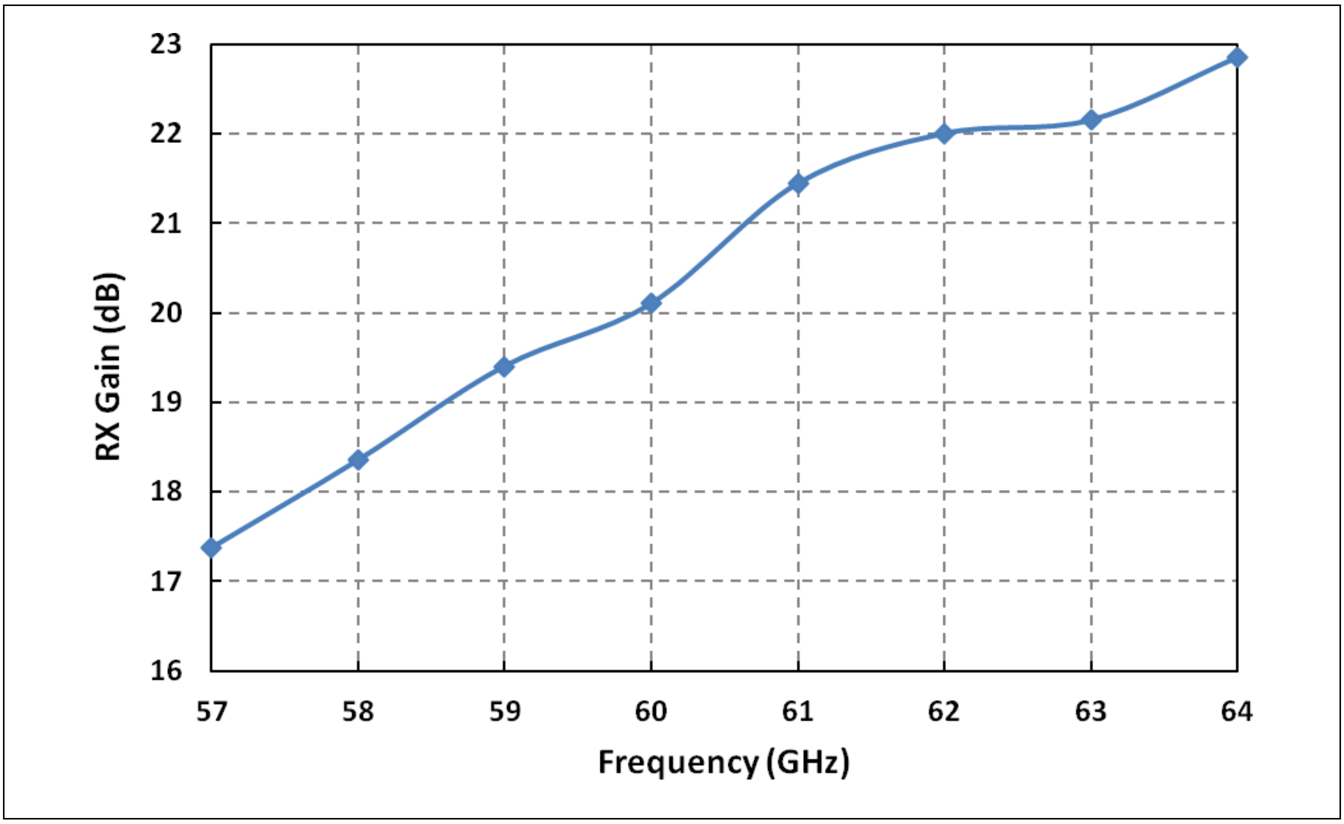


Figure 14 Receiver Gain over Frequency for BGT60

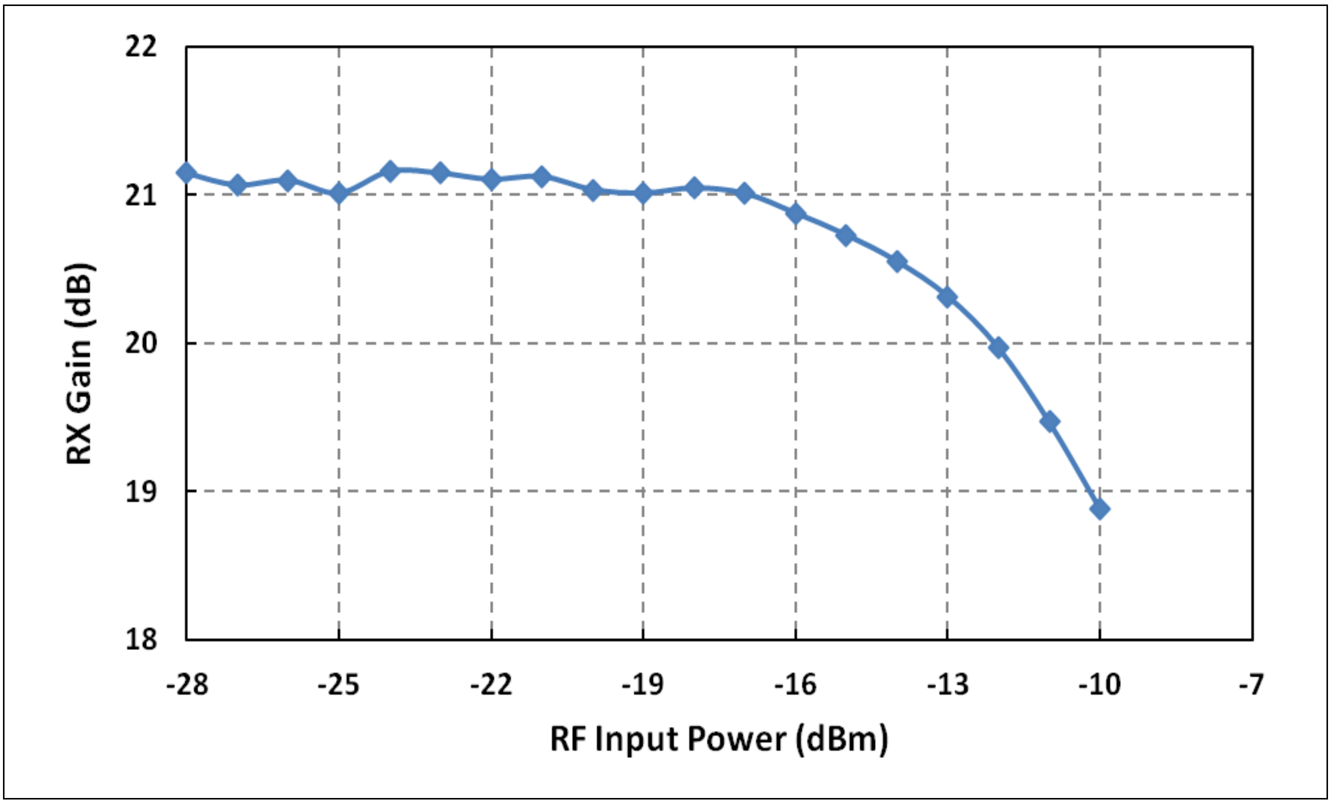


Figure 15 Input P1dB of Receiver @ f_{RX}=60 GHz

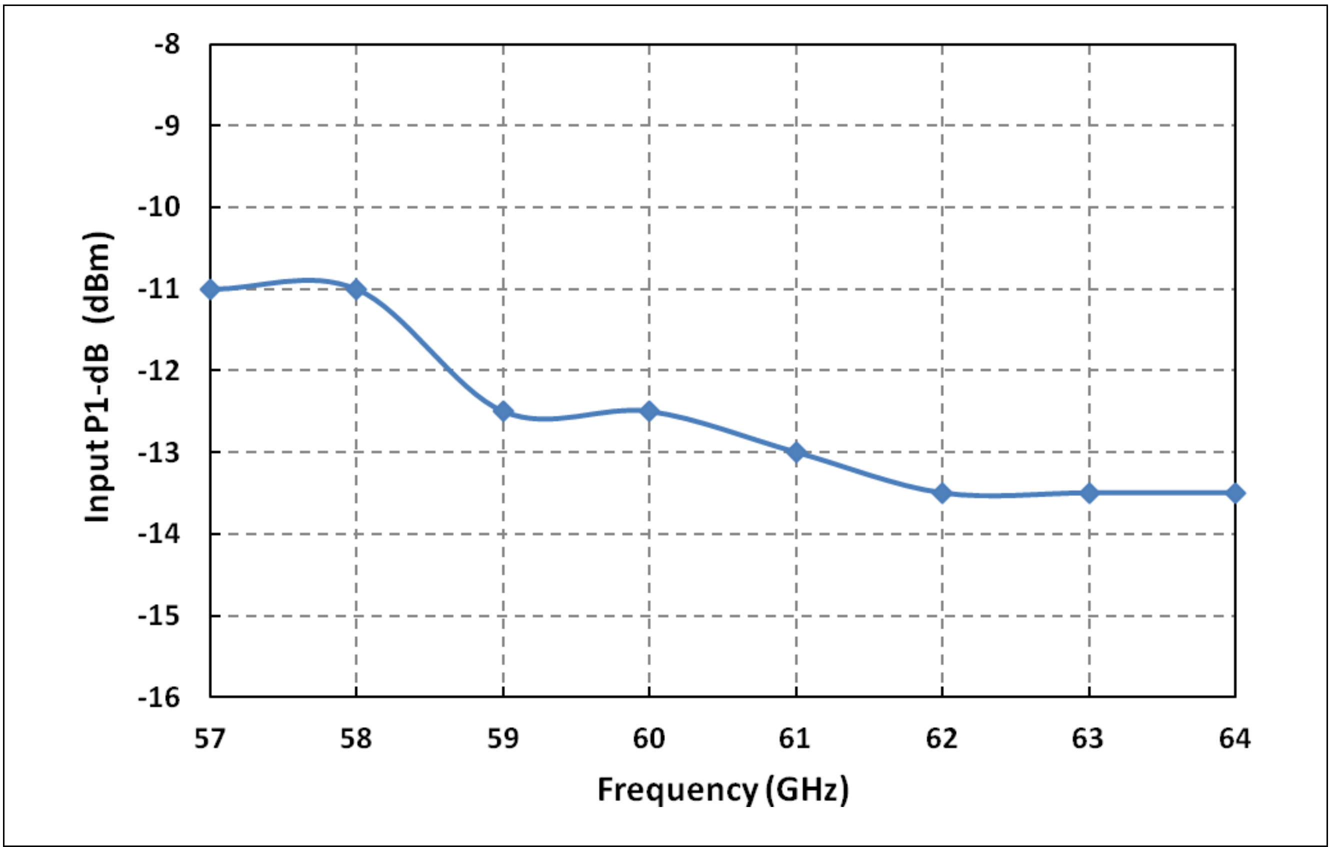


Figure 16 Input P1dB over Frequency of BGT60 Receiver

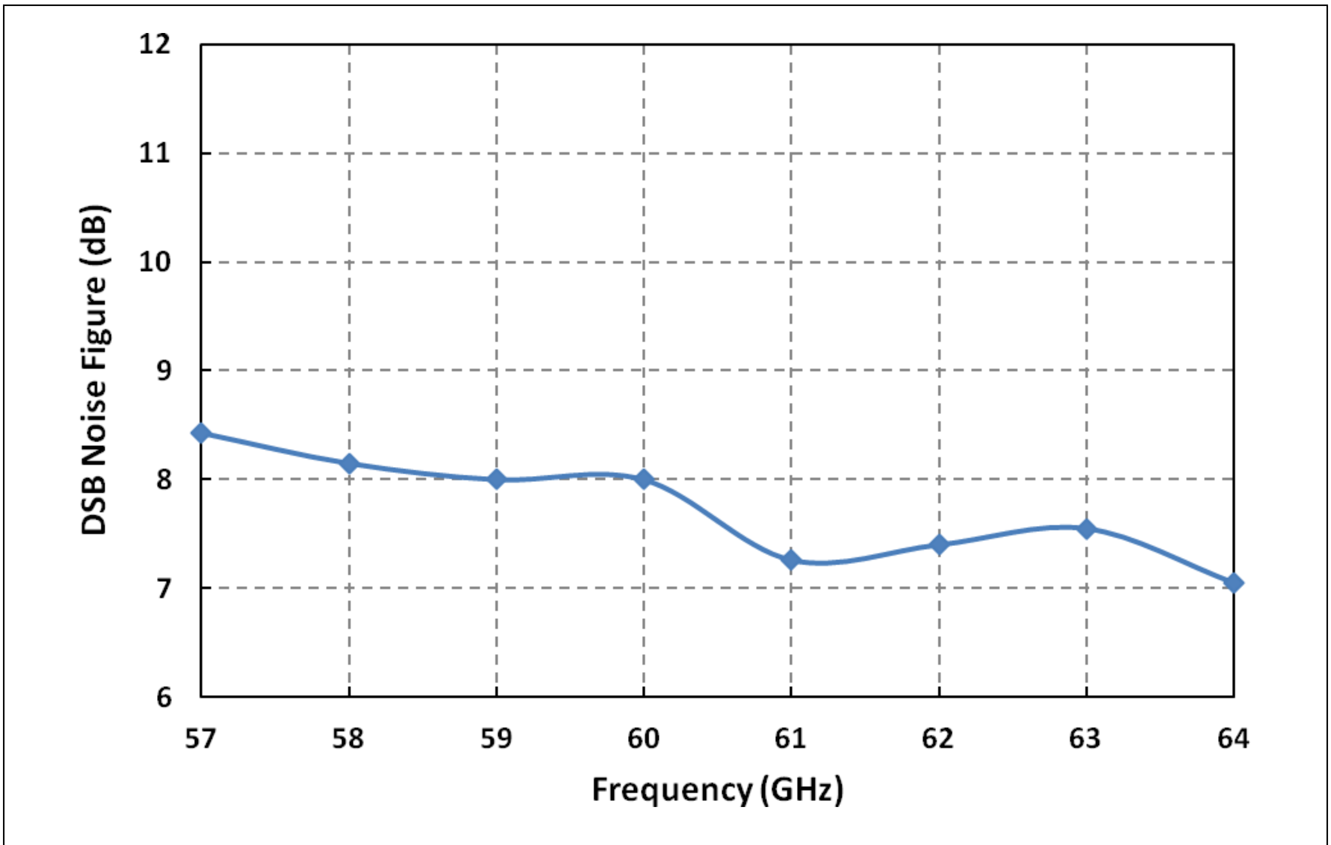


Figure 17 Noise Figure variation over Frequency for BGT60

8.1 Intercept Point Measurement of Receiver

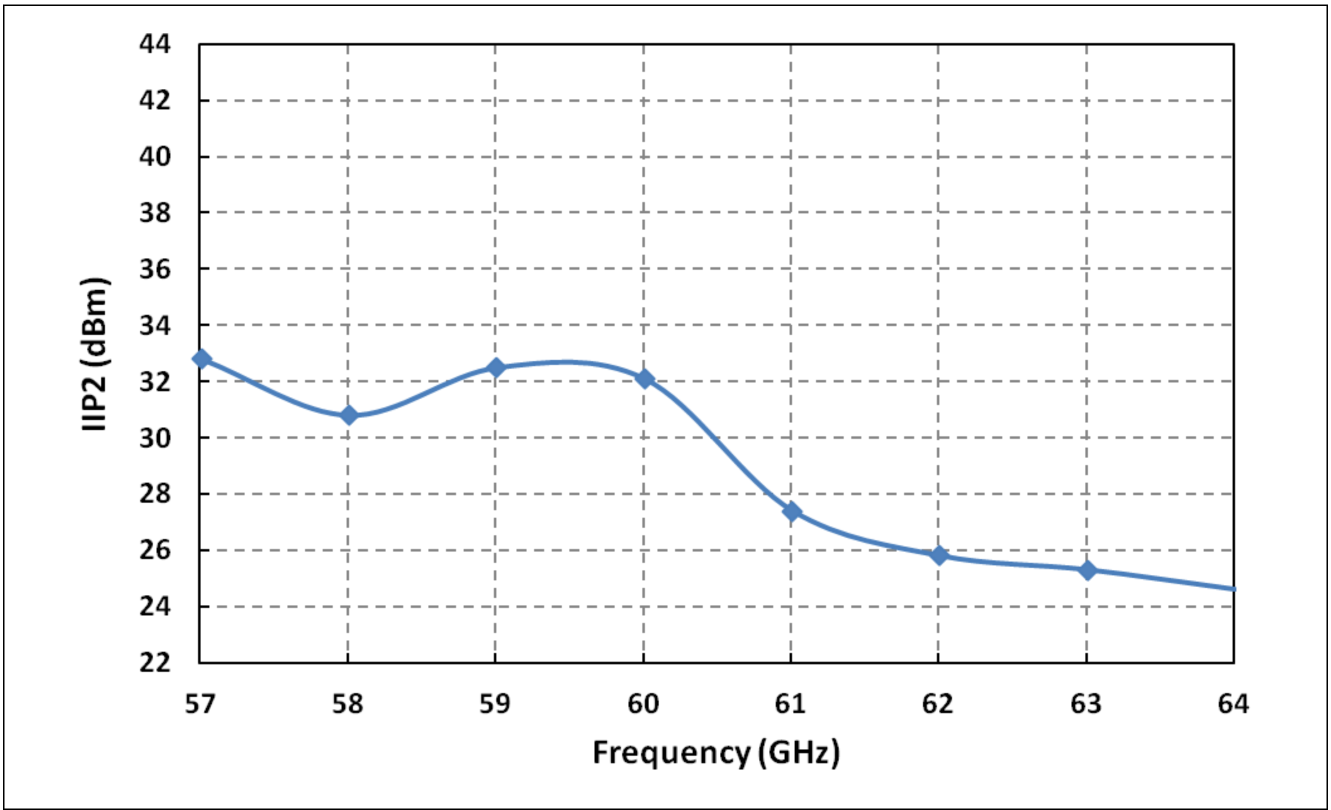


Figure 18 Input IP2 of Receiver over Frequency at $P_{RX\text{-}RF}$=-28 dBm

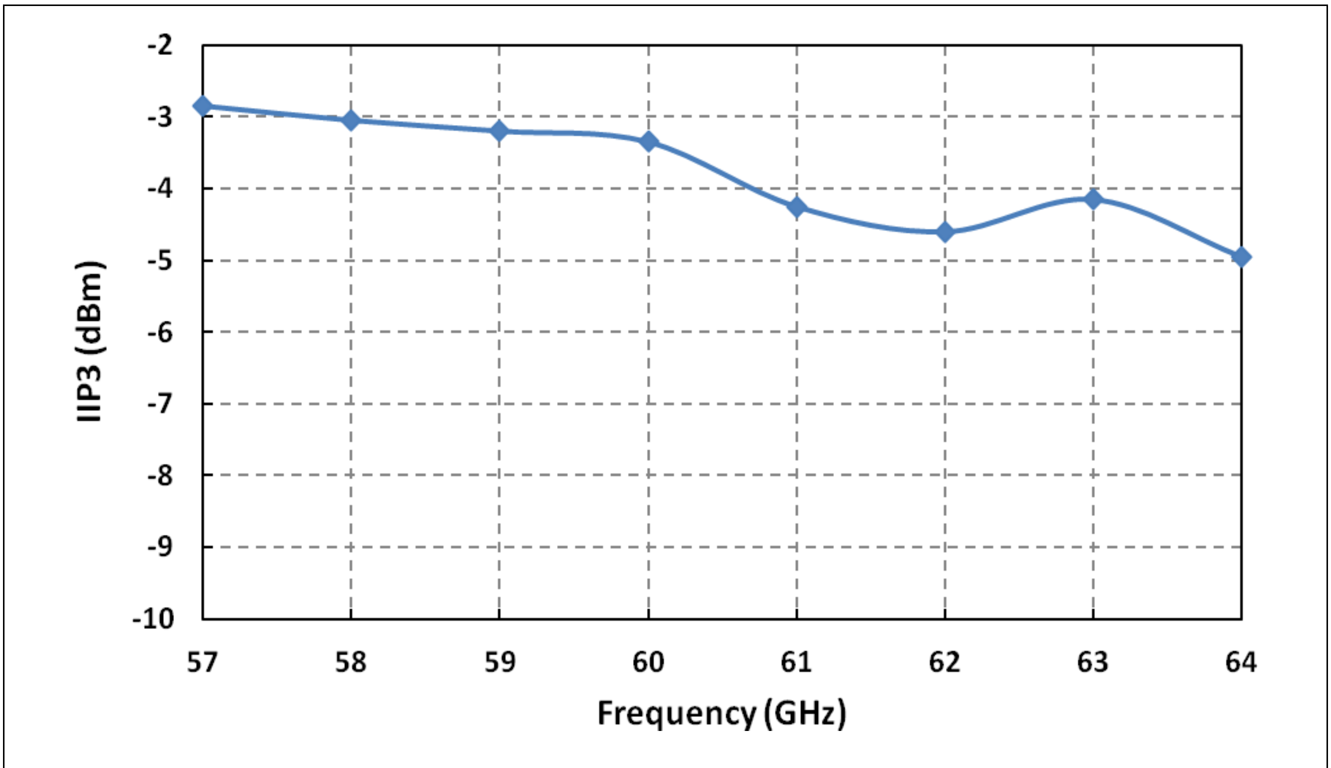


Figure 19 Input IP3 of Receiver over Frequency at $P_{RX\text{-}RF}$ = -30 dBm

9 VCO Signal Generation

BGT60 is designed to cover the complete tuning range of 57-64 GHz with 0-5.5 V of tuning voltage. All the chips are tested during production and VCO is centered with the help of divider output signal. **Figure 20** shows the tuning range of the VCO. The Tuning sensitivity (Kvco) is in the range of 5 GHz/V to 1.0 GHz/V (covering frequency 57-64 GHz) being higher at lower tuning voltages and lower at higher tuning voltages. The phase noise shown below is measured directly at TX port of the EVB.

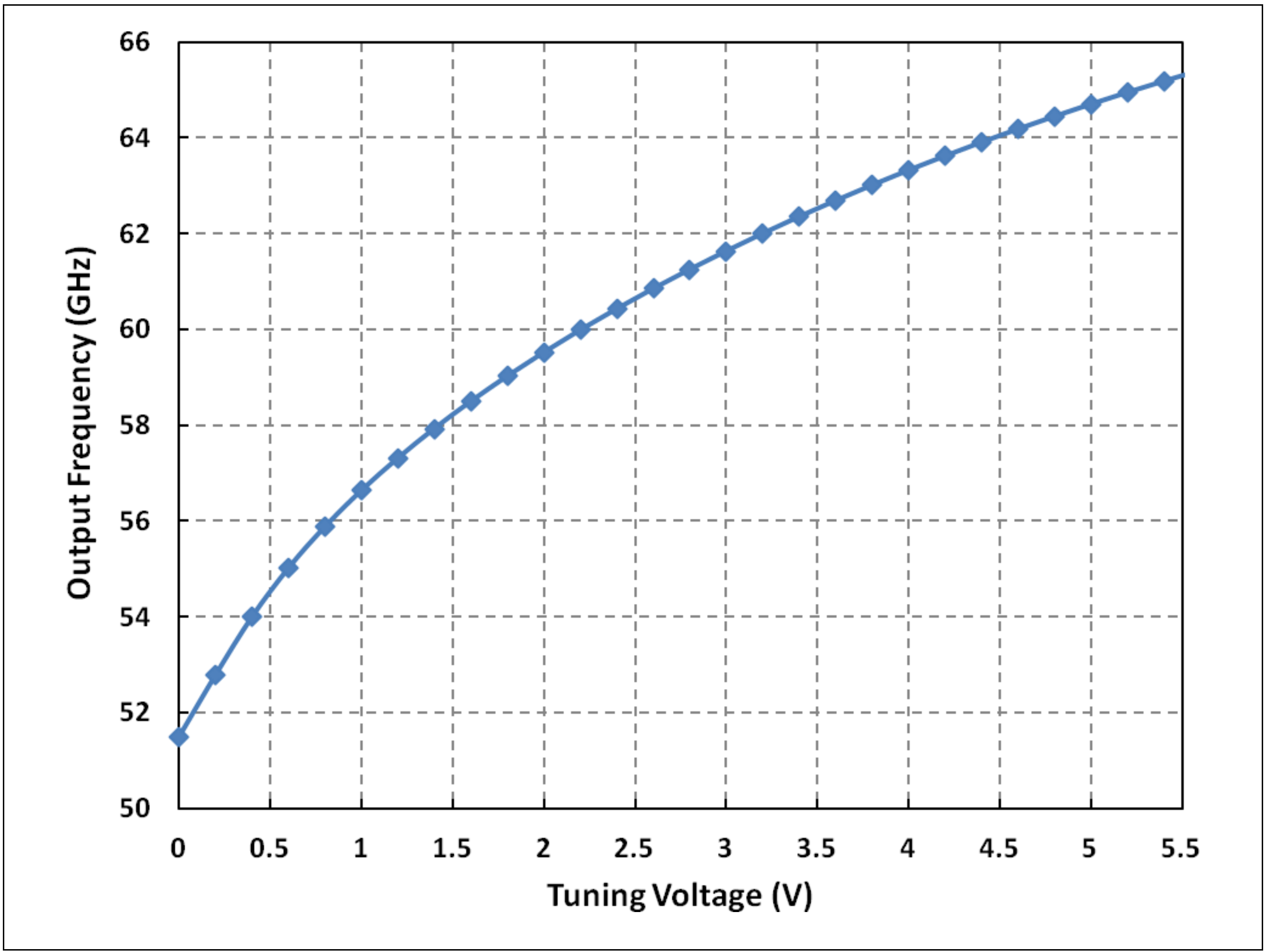


Figure 20 VCO Frequency over Tuning Voltage

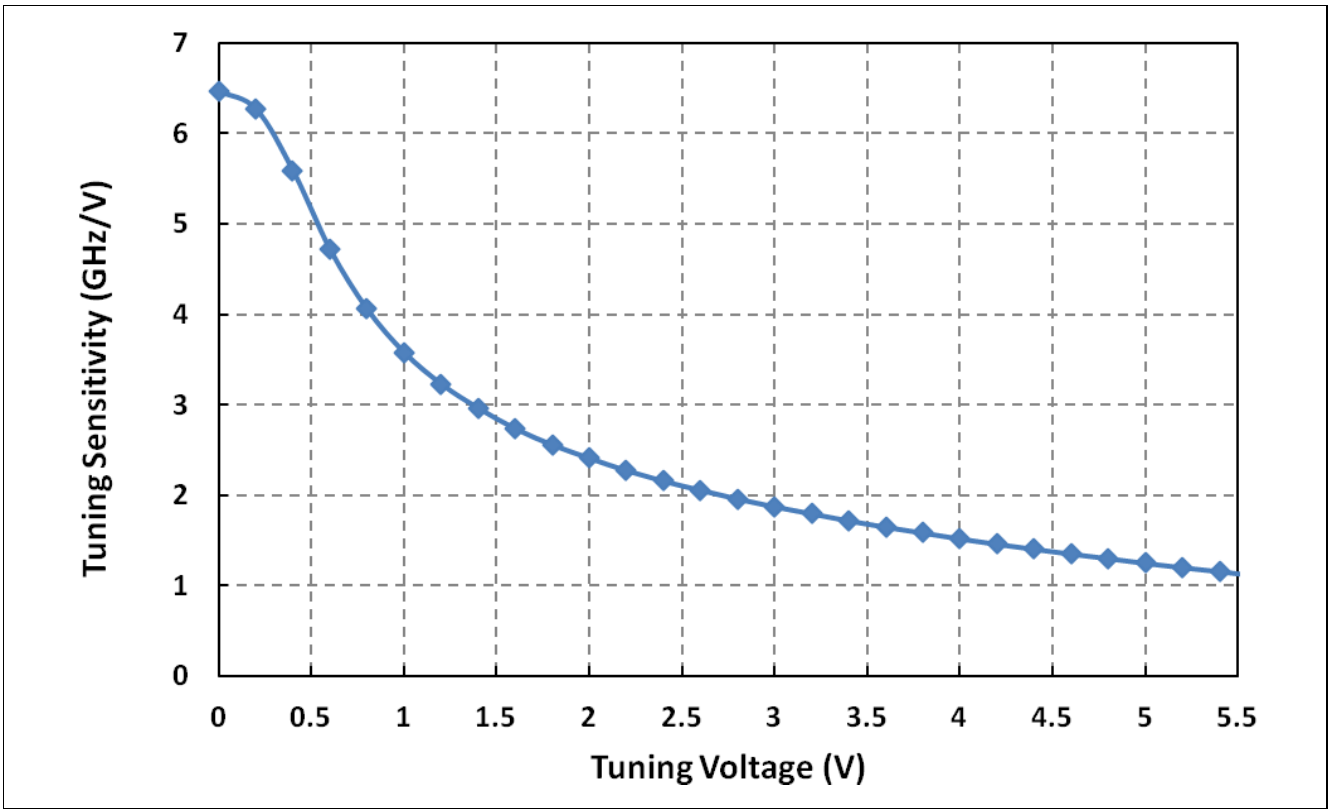


Figure 21 Tuning Sensitivity (Kvco) versus Tuning Voltage

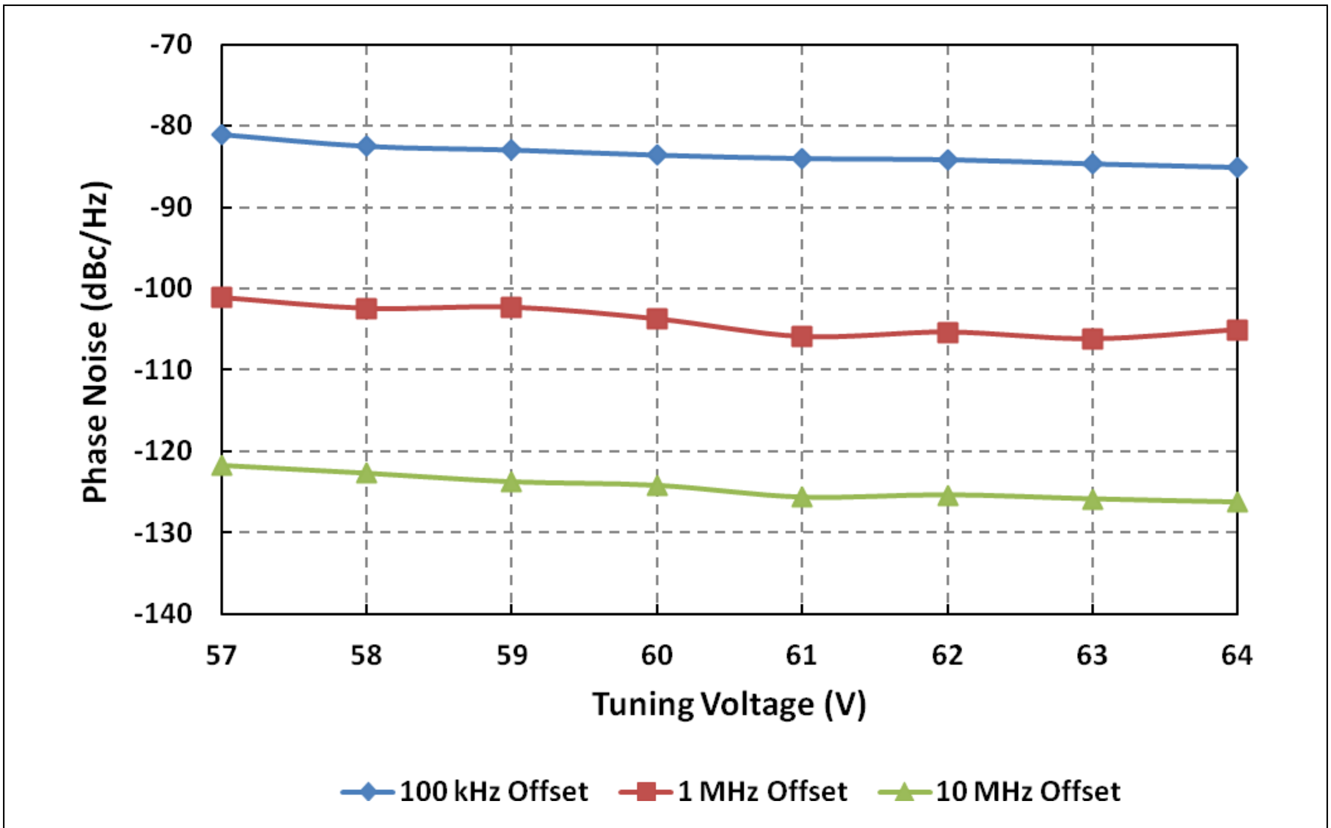


Figure 22 BGT60 Phase Noise Performance over Frequency

10 Getting Started with Evaluation Board

10.1.1 Configuring as Transmitter

To configure BGT60 as transmitter the following steps should be followed:

1) Apply Vcc=6V to the BGT60 board and connect USB cable from PC to the Evaluation Board. The current consumption should be in the range of 315 mA.
2) In the software folder supplied with this transceiver navigate to “E-Band V-Band SPI-Programmer.exe” and double click on it. A window will open as shown in **Figure 23** below.

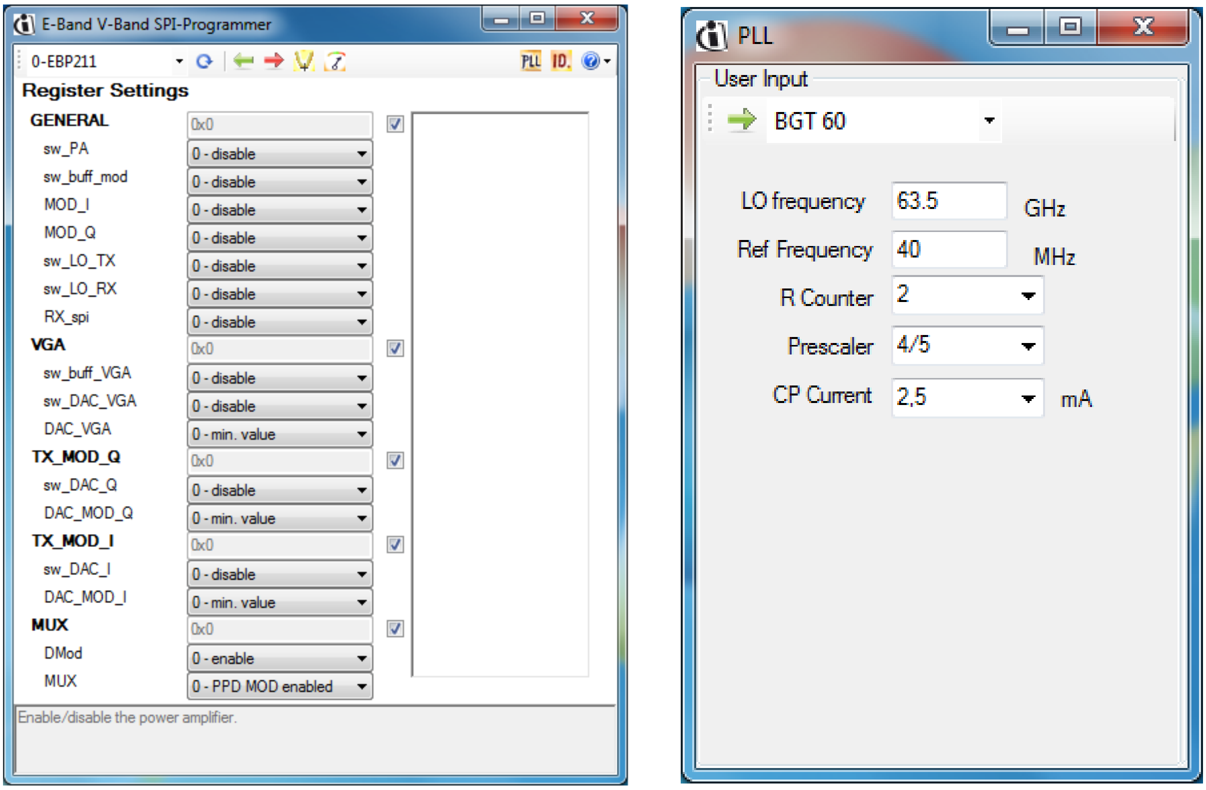


Figure 23 V-Band SPI-Programmer Main Window and PLL Window

3) Click on the “PLL” button on top right corner of this window. Another window will open which looks like **Figure 23**.
4) In this PLL window one can select the appropriate chip i.e. BGT60 or BGT70 or BGT80 from the drop down list. Then enter the required frequency in “LO frequency”.
5) In “Ref Frequency” box just enter the oscillation frequency of the reference used for PLL. In our case its 40 MHz reference. But exact frequency is also mentioned in the datalog or written on the backside of the board.

6) In "R Counter" box one can choose between different divider values >1. It should be noted that the PLL IC ADF4158, which is assembled on the Evaluation Board, accepts maximum PFD frequency of 32 MHz. "Prescaler" should be set to 4/5 and "CP Current" can be set to 2.5 mA. "CP Current" value will change the bandwidth of the loop filter used on the board.

7) After setting everything one should click on the "Green Arrow" in top left side of the PLL window.

8) Before you proceed to this step make sure that there is **no IF signal applied to the TX IF inputs**. Then in the main window press button. This step will automatically execute the LO leakage calibration and set the right value to the **DAC_MOD_Q** and **DAC_MOD_I** registers. The current consumption in this case will jump to 550mA. The typical setting for the Transmitter would look like as shown in **Figure 24**. After LO calibration is done, IF can be applied to TX IF inputs of BGT60.

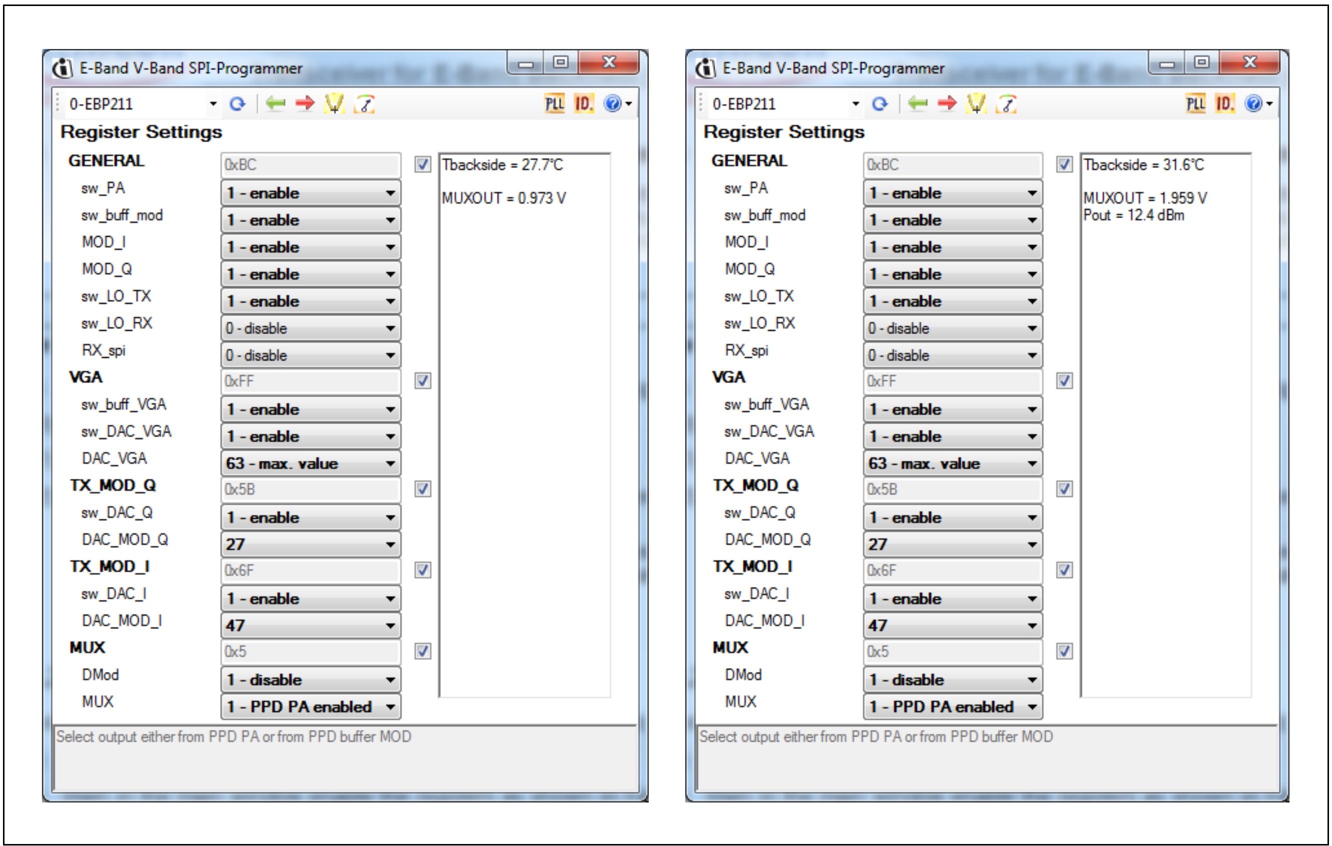


Figure 24 Typical Transmitter Settings for the BGT60

9) Pressing the "Red Arrow" button will update the chip temperature i.e. reading of the integrated temperature sensor and also display DC voltage at Muxout. The DC voltage at Muxout corresponds to the reading of PPD PA or PPD MOD. One of them can be selected at a time from the drop down list under MUX register.

10) Pressing the "Meter" button this button will give you the approximate power output of the device at its landing pad, when IF is applied on the TX input. The measurement is accurate up to -5 dBm of

output power. The power at the output of the transmitter can be controlled by changing the value of DAC_VGA register.

10.1.2 Configuring as Receiver

To configure BGT60 as receiver the following steps should be followed:

1) Follow step 1 to 7 from the above **Section 10.1.1**
2) Then in the main window enable the registers as shown in **Figure 25**. The supply current will jump to 427 mA.

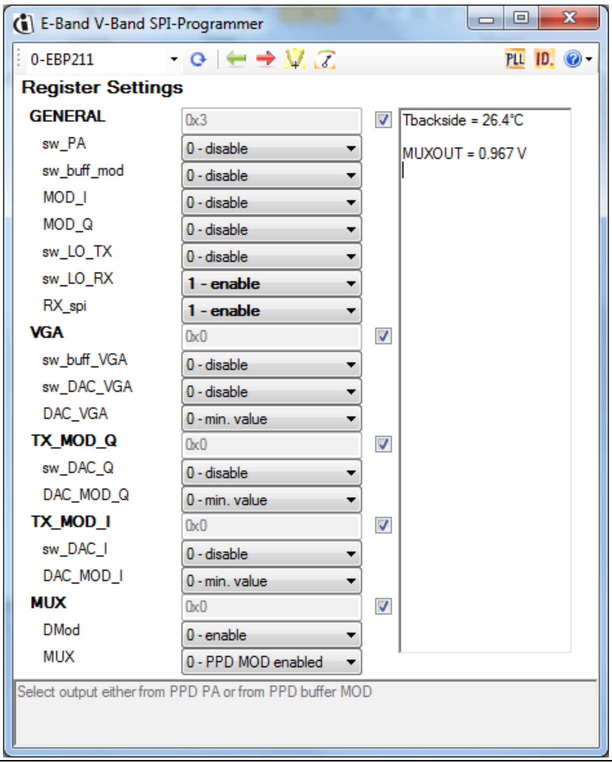


Figure 25 Typical Receiver Settings for BGT60

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